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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,145	02/07/2002	Guy E. Averett	ONS00317	1448

7590 07/25/2008

ON Semiconductor
Patent Administration Dept - MD A700
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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
07/25/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/072,145	AVERETT ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *34-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *34-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 34 and 38-41, are rejected under 35 U.S.C. 102(e) as being anticipated by Lur et al. (5,640,041).

Lur et al. teach in figures 10 and 14 and related text an intermediary of a semiconductor device, comprising:

a semiconductor substrate 10 formed with a first recessed region having a lower surface depressed with respect to a major surface of the semiconductor substrate;

a pillar region (the regions which includes pillars 24) comprising a silicon dioxide dielectric material formed in the first recessed region and extending from the lower surface, wherein a void region 8 is formed within the

pillar region; and

a polysilicon cap layer 5 formed overlying all upper surfaces of the pillar region and aligned (vertically aligned) with the void region, wherein sidewall surfaces of the pillar region are devoid of the polysilicon cap layer, and wherein the pillar region, the

polysilicon cap layer and the void region are configured to form an isolation region having reduced substrate capacitance.

Regarding claims 39-41, Lur et al. teach in figure 10 and related text the pillar region comprises a matrix of pillars 24, wherein at least a portion of the matrix of pillars includes pillars having a generally rectangular shape, and wherein the pillar region comprises a contiguous matrix.

Regarding claim 38, the claimed limitations of a pillar region comprises deposited silicon dioxide, these are process limitations which would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 35-37 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lur et al.

Regarding claim 35, Lur et al. teach substantially the entire claimed structure, as recited in claim 34, except explicitly stating that the polysilicon cap layer has a thickness of about 4,500 angstroms. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the polysilicon cap layer having a thickness of about 4,500 angstroms in prior art's device in order to reduce the size of the device.

Regarding claim 36, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to recess the upper surfaces of the pillar region below the major surface of the semiconductor substrate, in prior art's device in order to adjust the characteristics of the device according to the requirements of the application in hand.

Regarding claim 37, Lur et al. do not state that the upper surfaces are recessed a distance of about 0.5 microns. It would have been obvious to a person of ordinary skill

in the art at the time the invention was made to form the upper surfaces recessed a distance of about 0.5 microns in prior art's device in order to adjust the characteristics of the device according to the requirements of the application in hand.

Regarding claim 42, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form pillar region extending a distance of about 4.5 micrometers from the lower surface and has a dielectric constant of about 3.5 in prior art's device in order to reduce the size of the device and in order to adjust the characteristics of the device according to the requirements of the application in hand, respectively.

Response to Arguments

Applicant argues that figure 14 of Lur is not an intermediary.

Figure 14 of Lur does not depict voltage connections and additional external connections to the structure. For at least these reasons, figure 14 of Lur is an intermediary.

Applicant argues that "gate layer 5 is not configured to form an isolation region having reduced substrate capacitance", because "It merely sits on top of Lur's isolation region, but plays no part whatsoever in the formation of it.

Applicant's structure comprising a polysilicon cap layer sitting on top of an isolation region and having reduced substrate capacitance. Lur et al. also teach a structure comprising a polysilicon cap layer sitting on top of an isolation region. Therefore, Lur et al.'s structure also has a reduced substrate capacitance.

Applicant argues that Lur et al. do not teach a poiysilicon cap layer overlies all upper surfaces of the pillar region, because "As is clear in FIG. 14, gate layer 5 only overlies a portion of the finished isolation region".

Lur et al. teach a poiysilicon cap layer overlies all upper surfaces of the pillar region, because there are no upper surfaces of the pillar region which are located above the poiysilicon cap layer.

Applicant argues that Lur et al. do not teach a polysilicon cap layer aligned with the void region, because "Gate layer 5 in FIG. 14 is clearly not so oriented".

The broad recitation of the claim does not require the lower surface of the polysilicon cap layer is aligned with the upper surface of the void region. Clearly, figure 14 of Lur et al. depicts the polysilicon cap layer being vertically aligned with the void region. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
7/25/2008

/ORI NADAV/
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